Amendments to the Specification

Please amend the last two paragraphs on page 13 as follows:

Figs. 9A through 20 A and 22A show top views of the process flow proposed in the second preferred embodiment of the present invention.

Figs. 9B through 20B, Fig. 21, and Fig.22B show cross-sectional views along A-A' of Fig. 9A of the process flow proposed in the second preferred embodiment of this invention.

Please amend the first paragraph on page 14 as follows:

Figs. 9C to Fig. ~~21C~~ 20C show cross-sectional views along B-B' of Fig. 9A of the process flow proposed in the second preferred embodiment of this invention.

Please amend the third paragraph of page 3 as follows:

~~Fig. 32 is a top view representation of the fourth preferred embodiment array structure of the present invention.~~

Please amend the paragraph bridging pages 26 and 27 as follows:

There are three more variation in the fabrication method of the second embodiment. The 1st variation is to define the CG hard mask 114 after cap nitride strip as shown in Fig. 21B instead of the step after cap nitride mask described in Fig. 10B. CG mask 114 does not have to be oxide.

Please amend the paragraph bridging pages 29 and 30 as follows:

A top view and a cross sectional structure of the fourth embodiment are shown in Fig.30A and Fig.30B. It is simply replacing the floating gate in the conventional NAND by nitride 312 besides reducing the cell size. The memory cell structure is of subtracting the word gate 242 in Fig.23B of the third embodiment and forming a diffusion area instead. The unit cell is shown in Fig.30 as a rectangular dotted line. It consists of a half of a diffusion area combining memory LDD 302 and source/drain 303, a control gate with underlying ONO 311/312/313 as a memory storage and the other half of the diffusion area along the channel direction. Crossing direction is bounded by conventional STI 310. The oxide sidewall mask 314 defines the width of the control gate and underlying ONO to between about 30nm and 60nm. It is much smaller than the control gate width of the conventional NAND. The direction across the channel is bounded by STI along the channel. The array structure follows NAND with the only difference being replacing the floating gate by nitride. The bit lines run along the active area isolated by STI lines. The control gate lines are across the bit lines. An operation block is defined as a (n bit lines x m control gate lines) matrix. The control gate lines 370B ,

370S at both ends of the block are assigned as gates to select a block to be operated. Two adjacent blocks share a diffusion area in between either as a common source line adjacent to the select gate 370S or a data bit adjacent to the other select gate 370B connecting to a bit line 351 through a contact 350. The control gate mask 314 is a sidewall image. The sidewall image loops around ~~as shown in Fig.32~~. The looping mask is separated into two lines by cutting it at both ends. The adjacent control gate lines of adjacent loops are cut at the control edge cut 381 alternately each end ~~as shown in Fig.32~~. The control gate contact cover 380 is placed on the out side of edge cut 381.

Amendments to the Drawings

The attached proposed sheet of drawings includes changes to Fig. 21B and replaces the original drawing sheet of Figs. 21B, 22A, 22B, and 22C. Fig. 21B has been renumbered to be Fig. 21.

Attachments: Replacement sheet

Annotated Sheet Showing Changes